RCE / DAQ possibilities at NYU

Andy Haas
SLAC → NYU

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SLAC NATIONAL ACCELERATOR LABORATORY

NEW YORK UNIVERSITY

ATLAS

Intro to RCE

- SLAC-designed board(s) for versatile and efficient DAQ

- Fast and cheap
- Modern high-level programming languages
- Modular

- Generic computing elements, FPGA/DSP/CPU → “RCE”
- High bandwidth interconnects → 10 Gb ethernet
- Modern crate support → ATCA

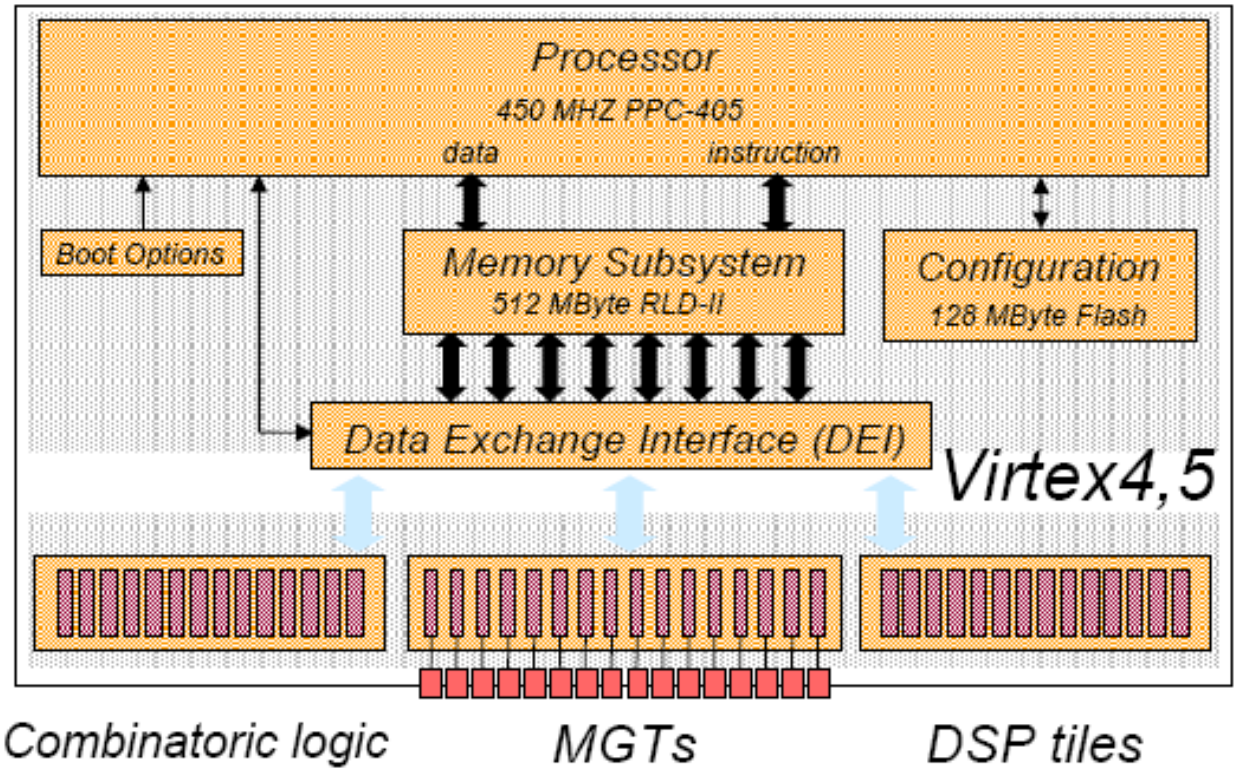
- Can be a “ROD”
- Can be a “ROS”
- Can do both at once, and can do more...
  (triggering? pre-processing?)

Reconfigurable Cluster Element (RCE)

Modern design for high-rate data manipulation and transfer

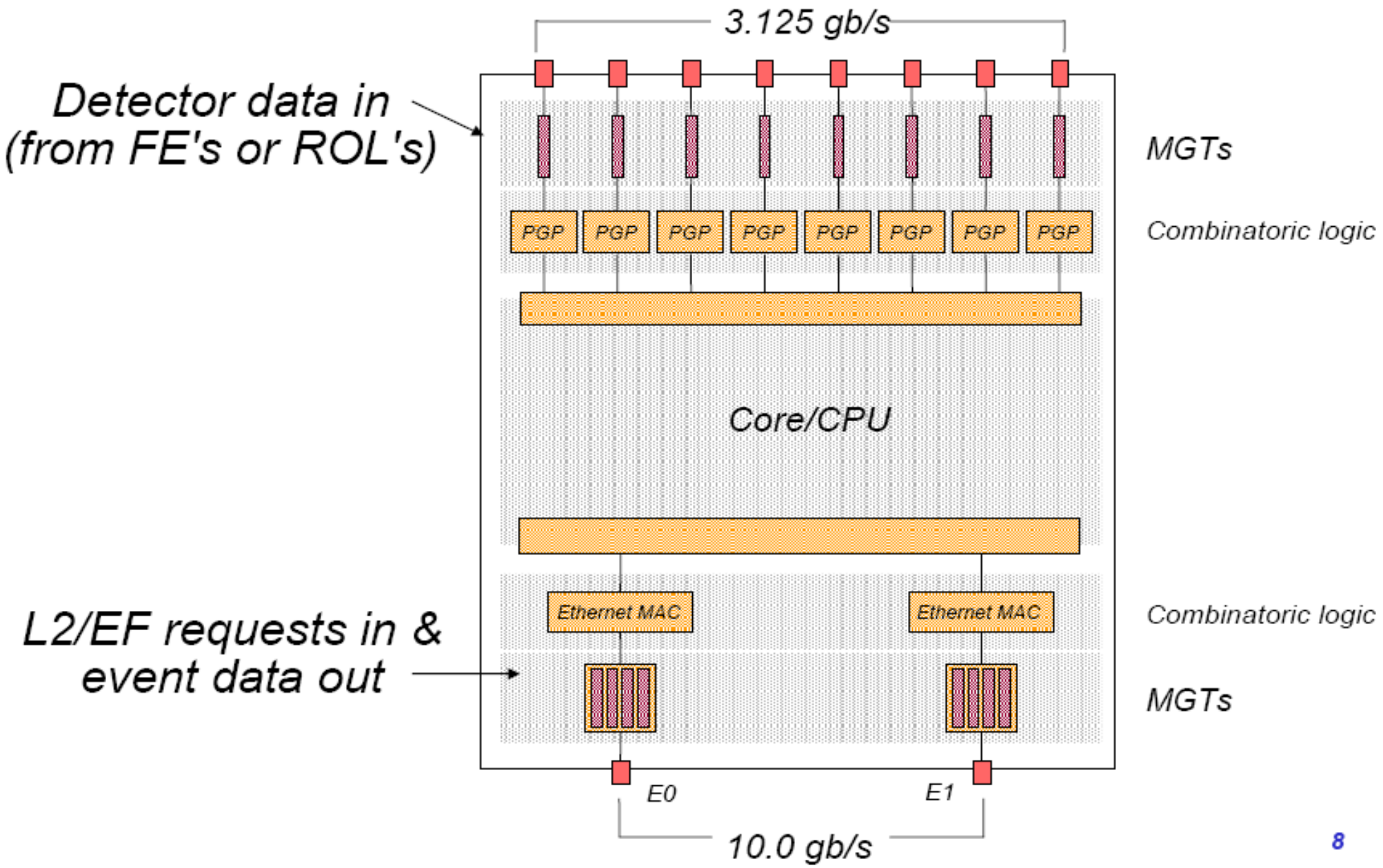
Easy to use/program, relatively cheap

~10 Gb/s in & out

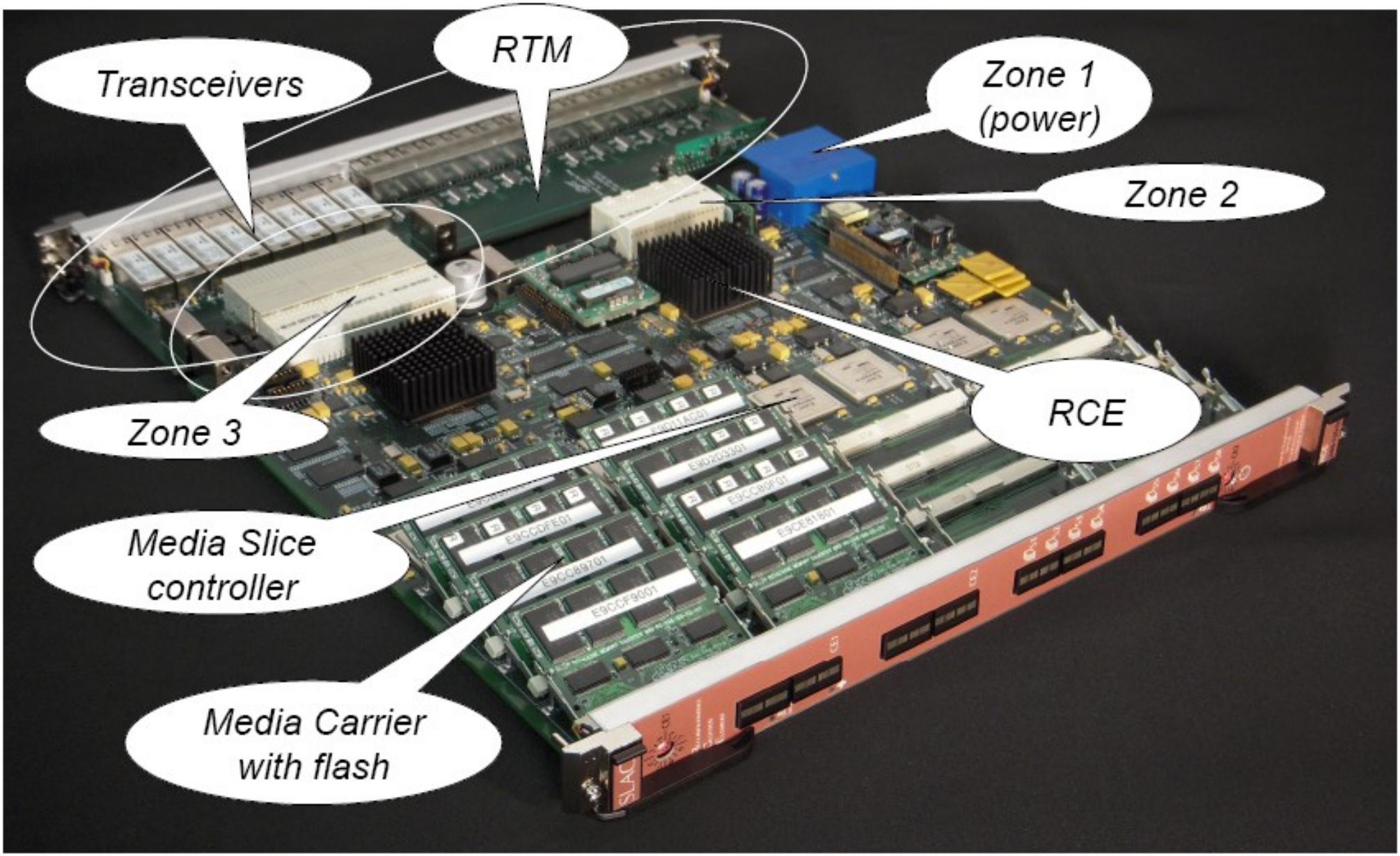


- **Bundled software:**
  - GNU cross-development environment (C & C++)
  - remote (network) GDB debugger
  - network console
- **Bundled software:**
  - bootstrap loader
  - Open Source kernel (RTEMS)
    - POSIX compliant interfaces
    - standard I/P network stack
  - exception handling support
- **Class libraries (C++) provide:**
  - DEI support
  - configuration interface

Example RCE Configuration

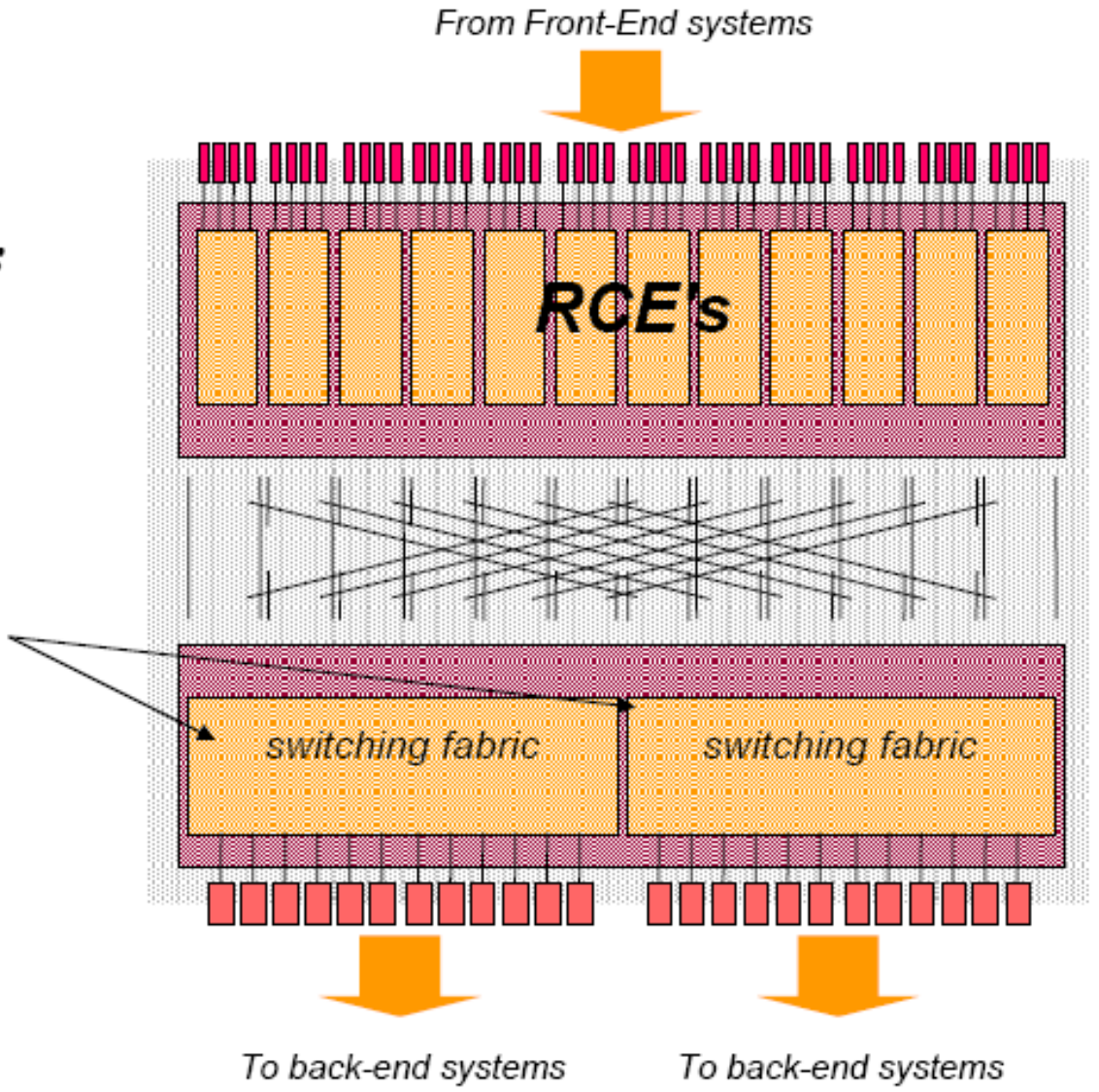


Demo RCE board + RTM

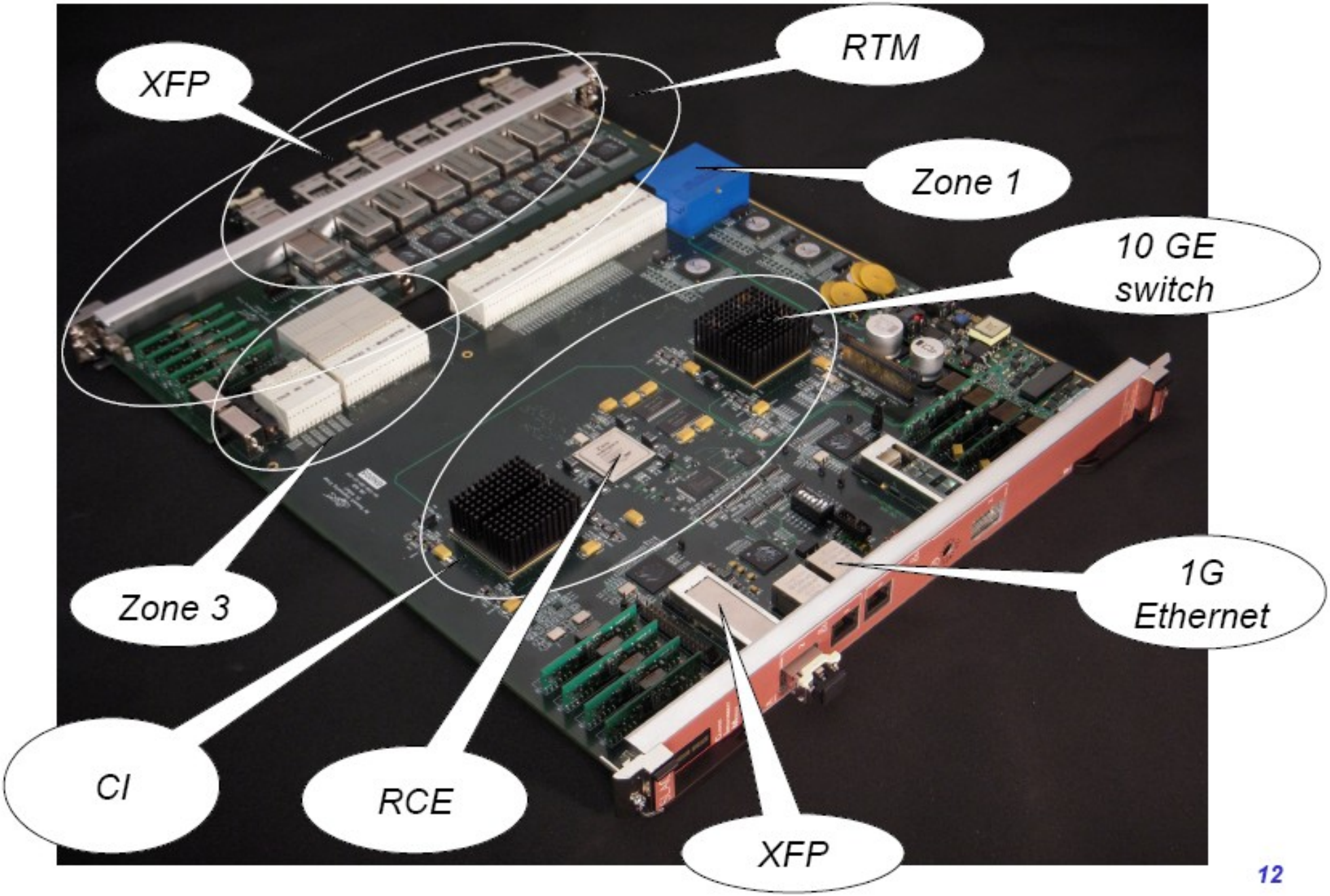


The Cluster Interconnect (CI)

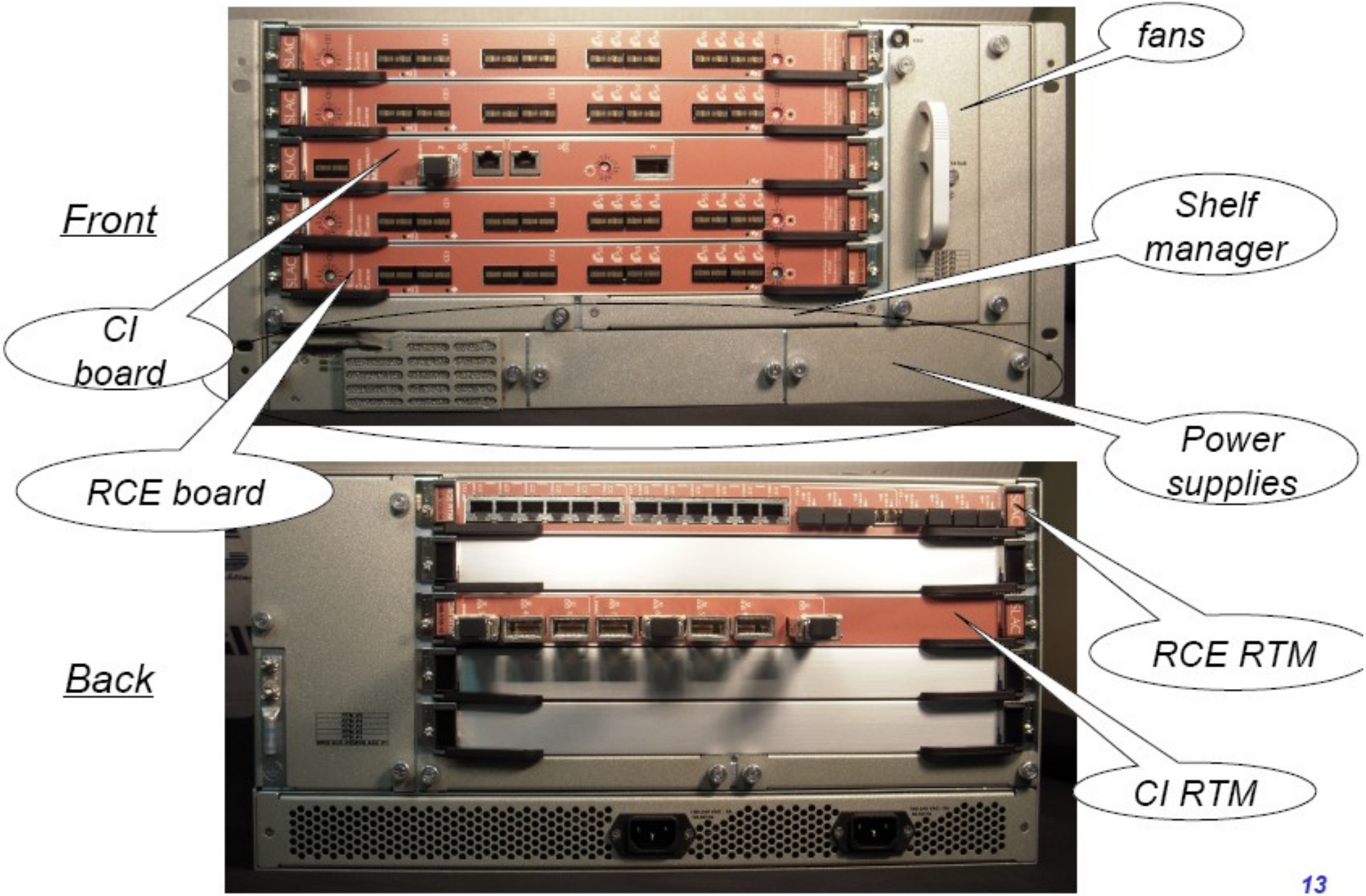
- Connects RCE's together
  - High bandwidth, low latency
- Based on two Fulcrum FM224s
  - 24 port 10-GE switch
  - Packet latency <200 ns



Demo Cluster Interconnect board + RTM

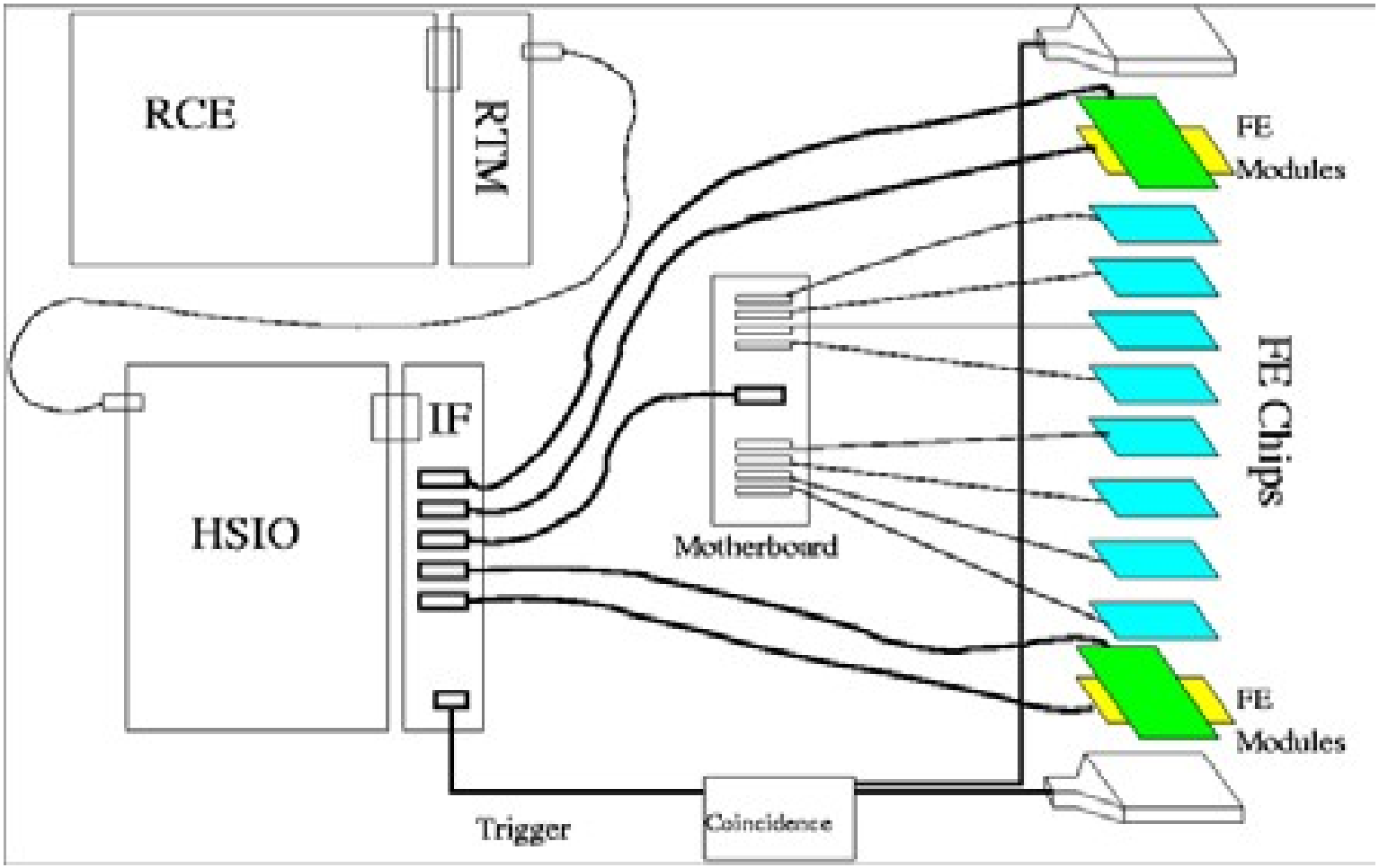


Demo (5 slot) ATCA crate



Tests at SLAC

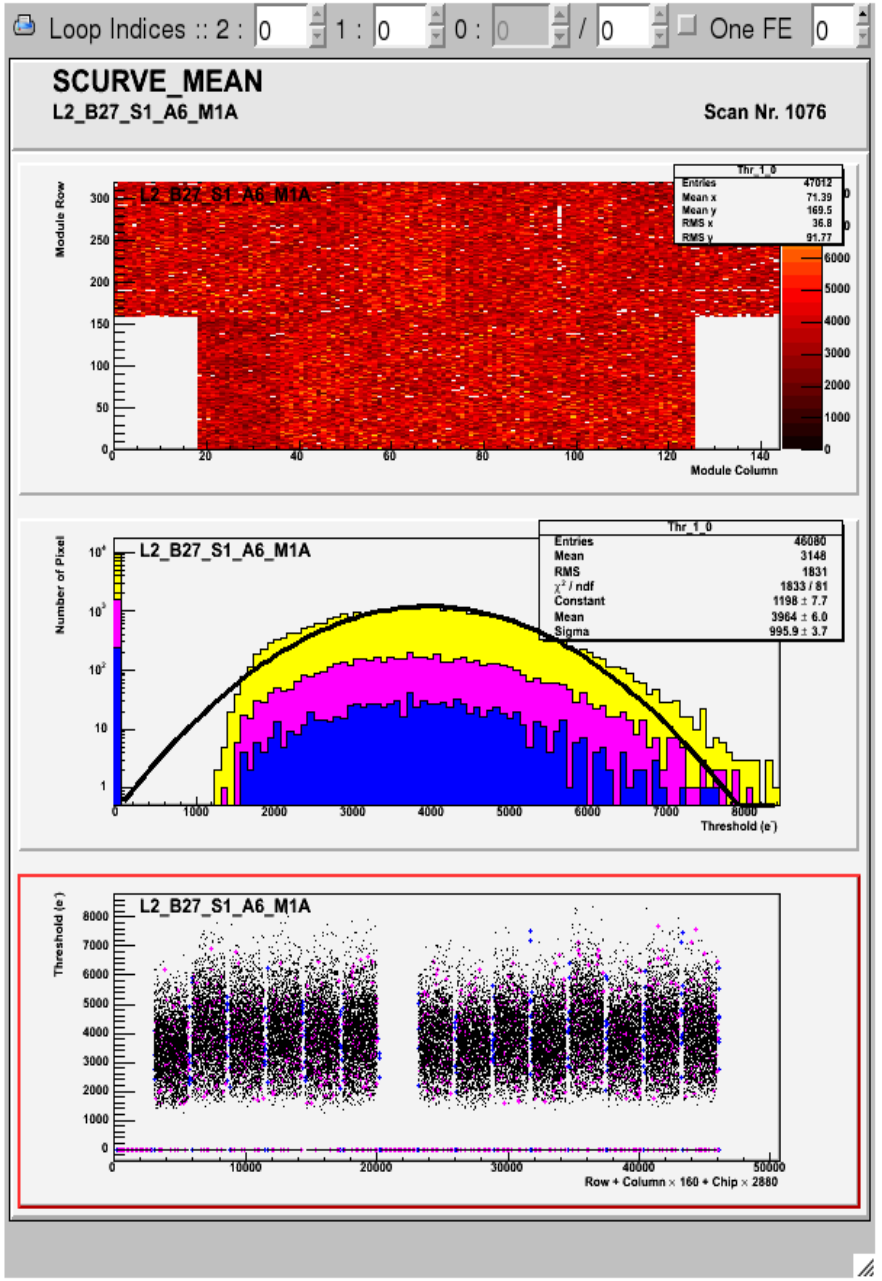
- Pixel readout (FE-I3 and FE-I4) and calibration
- In future: HSIO will be RCE-based, integrated TTCrx chip on RCE



Tests at SLAC

- Much faster DAQ and calibration than standard ATLAS ROD / VME infrastructure
- Software ported with relative ease

- In future: use DSPs for fits



Interested Groups

Collaborators (group PIs underlined):

Argonne National Laboratory:

Robert Blair, Jinlong Zhang

University of California, Irvine:

Andrew Lankford, Raul Murillo Garcia

Michigan State University:

Wade Fisher, Reiner Hauser, Reinhard Schwienhorst, Kirsten Tollefson

University of Oregon:

Nikolai Sinev, David Strom, Eric Torrence

SLAC National Accelerator Laboratory:

Rainer Bartoldus, Ric Claus, Andy Haas, Gunther Haller, Ryan Herbst, Mike Huffer, Martin Kocian, Chris O'Grady, Jim Panetta, Amedeo Perazzo, Emanuel Strauss, Steve Tether, Gregg Thayer, Dong Su, Matt Weaver, Matthias Wittgen

Stony Brook University:

Erik Devetak, David Puldon, Dmitri Tsybychev

University of Washington:

Gordon Watts

University of Wisconsin:

Werner Wiedenmann, Saulan Wu, Haimo Zobernig

Yale University

Sarah Demers

and of course now NYU… !

Future R&D at NYU

- Tests of readout and calibration of pixel / strip silicon
  - RTMs, optical readout links
- Programming of DSP tiles for fitting etc.
- RCE and HSIO software development
- Tests of communication between RCE's
  - UDP / TCP functionality
  - Triggering (fixed latency)
  - Bandwidth
- ROS emulation …

- Clear potential for collaboration with silicon R&D
  - RCE-based test-stands for high-speed tests and calibrations
  - Sources of real data for testing of RCE DAQ hardware and software